BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Abdelilah et al.	:	Before the Examiner: Moore, Patrick M.
Serial No.: 10/783,757	:	Group Art Unit: 2188
Filing Date: February 20, 2004	:	
Title: FACILITATING INTER-DSP DATA COMMUNICATIONS	:	IBM Corporation IP Law Dept. YXSA, Bldg. 002 3039 Cornwallis Road P.O. Box 12195 Research Triangle Park, NC 27709

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-30 are pending in the Application. Claims 1-30 stand rejected. Claims 1-30 are appealed.

IV. STATUS OF AMENDMENTS

Appellants have not submitted any amendments following receipt of the final office action with a mailing date of November 7, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1:

In one embodiment of the present invention, a method for facilitating inter-digital signal processing (DSP) data communications comprises the step of reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, where the first data structure comprises a first source address indicating a first address of where data is stored in the local memory of the first DSP processor core, where the first data structure further comprises an indication of a size of a block of memory, where the first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core. Specification, page 18, line 26 – page 20, line 6; Specification, page 25, lines 11-19; Specification, page 32, lines 15-18; Specification, page 40, lines 1-4; Figure 7, element 700; Figure 9, step 902; Figure 12, step 1202; Figure 15, step 1502. The method further comprises initiating a transfer of moving data the size of the block of memory located in the first source address in the local memory of the first DSP processor core to the first destination address in the local memory of the second DSP processor core. Specification, page 26, lines 7-11; Specification, page 33, lines 5-9; Specification, page 40, lines 18-22; Figure 9, step 904; Figure 12, step 1204; Figure 15, step 1504.

Independent Claim 11:

In another embodiment of the present invention, a computer program product embodied in a machine readable medium for facilitating inter-digital signal processing (DSP) data communications comprises the programming step of reading a

first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, where the first data structure comprises a first source address indicating a first address of where data is stored in the local memory of the first DSP processor core, where the first data structure further comprises an indication of a size of a block of memory, where the first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core. Specification, page 11, line 20 – page 12, line 14; Specification, page 18, line 26 – page 20, line 6; Specification, page 25, lines 11-19; Specification, page 32, lines 15-18; Specification, page 40, lines 1-4; Figure 7, element 700; Figure 9, step 902; Figure 12, step 1202; Figure 15, step 1502. The computer program product further comprises the programming step of initiating a transfer of moving data the size of the block of memory located in the first source address in the local memory of the first DSP processor core to the first destination address in the local memory of the second DSP processor core. Specification, page 11, line 20 – page 12, line 14; Specification, page 26, lines 7-11; Specification, page 33, lines 5-9; Specification, page 40, lines 18-22; Figure 9, step 904; Figure 12, step 1204; Figure 15, step 1504.

Independent Claim 21:

In one embodiment of the present invention, a system comprises a plurality of digital signal processing (DSP) units. Specification, page 10, line 26 – page 12, line 14; Figure 3, elements 302. The system may further comprise a direct memory access controller coupled to the plurality of DSP processor cores, where the direct memory access controller comprises a memory unit operable for storing a computer program for facilitating inter-DSP data communications; and a processor coupled to the memory unit. Specification, page 10, line 26 – page 12, line 14; Figure 3, elements 204, 302. The processor, responsive to the computer program, comprises circuitry operable for reading a first data structure associated with a block of local memory in a first DSP processor core, where the first data structure comprises a first source address indicating a first address of where data is stored in the local memory of the

first DSP processor core, where the first data structure further comprises an indication of a size of a block of memory, where the first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core. Specification, page 11, line 20 – page 12, line 14; Specification, page 18, line 26 – page 20, line 6; Specification, page 25, lines 11-19; Specification, page 32, lines 15-18; Specification, page 40, lines 1-4; Figure 7, element 700; Figure 9, step 902; Figure 12, step 1202; Figure 15, step 1502. The processor further comprises circuitry operable for initiating a transfer of moving data the size of the block of memory located in the first source address in the local memory of the first DSP processor core to the first destination address in the local memory of the second DSP processor core. Specification, page 11, line 20 – page 12, line 14; Specification, page 26, lines 7-11; Specification, page 33, lines 5-9; Specification, page 40, lines 18-22; Figure 9, step 904; Figure 12, step 1204; Figure 15, step 1504.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-30 stand rejected under 35 U.S.C. §102(b) as being anticipated by So (U.S. Patent No. 6,148,389).

VII. ARGUMENT

The Examiner has rejected claims 1-30 under 35 U.S.C. §102(b) as being anticipated by So (U.S. Patent No. 6,148,389). Appellants respectfully traverse for at least the reasons stated below.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

A. Claims 1, 11 and 21 are not anticipated by So.

Appellants respectfully assert that So does not disclose "reading a first data structure associated with a block of local memory in a first DSP processor core in a

complex comprising a plurality of DSP processor cores" as recited in claim 1 and similarly in claims 11 and 21. The Examiner cites column 1, lines 44-50; column 2, lines 29-35 and Figure 21 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 2. Appellants respectfully traverse.

So instead discloses a PC system that includes a main CPU microprocessor, a file-based operating system, and a DSP microprocessor arranged so that the DSP can execute main CPU operations during time intervals in which the main CPU is otherwise occupied. Column 1, lines 44-48. So further discloses an integrated circuit having a DSP core, an interface circuit including a master/slave bus interface and a translation circuit, and a memory circuit comprising FIFO function coupled to the master/slave bus interface and a RAM function coupled to the translation circuit, and the DSP core is coupled to the memory and interface circuit. Column 2, lines 29-35. There is no language in the cited passages that discloses reading a data structure. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory in a DSP processor core. Neither is there any language in the cited passages that discloses reading a data structure associated with a block of local memory in a DSP processor core in a complex comprising a plurality of DSP processor cores. Thus, So does not disclose all of the limitations of claims 1, 11 and 21, and thus So does not anticipate claims 1, 11 and 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core" as recited in claim 1 and similarly in claims 11 and 21. The Examiner cites column 16, lines 8-18 and Figure 21 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 2. Appellants respectfully traverse and assert that So instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. So further discloses that the three addresses needed are the base address for the DSP's 128K

bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, So discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses a data structure that comprises a source address. Instead, the cited passage simply discloses that the CPU provides pointer addresses to the main memory, where the three addresses needed include the 128K bytes of read data space. Neither is there any language in the cited passage that discloses a data structure that comprises a source address indicating an address of where data is stored in the local memory of a DSP processor core. Thus, So does not disclose all of the limitations of claims 1, 11 and 21, and thus So does not anticipate claims 1, 11 and 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "wherein said first data structure further comprises an indication of a size of a block of memory" as recited in claim 1 and similarly in claims 11 and 21. The Examiner cites the phrase "regions cannot exceed 128KB" in Figure 25 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 2. Appellants respectfully traverse. This statement is related to the size limitations of the scatter locked regions in a destination data DMA transfer table structure. This is not the same as having a data structure, associated with a block of local memory in a DSP processor core, that includes an indication of a size of a block of memory. Thus, So does not disclose all of the limitations of claims 1, 11 and 21, and thus So does not anticipate claims 1, 11 and 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core" as recited in claim 1 and similarly in claims 11 and 21. The Examiner cites column 16, lines 8-18 and Figure 21 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 2. Appellants respectfully traverse. As stated above, So

instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. So further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, So discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses a data structure, associated with a block of local memory in a DSP processor core, that includes a destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core. Thus, So does not disclose all of the limitations of claims 1, 11 and 21, and thus So does not anticipate claims 1, 11 and 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core" as recited in claim 1 and similarly in claims 11 and 21. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 3. Appellants respectfully traverse and assert that So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of moving data the size of the bock of memory located in the first source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of moving data the size of the bock of memory located in the first source address in the local memory of the first DSP processor core to the destination address in the local memory of the second DSP processor core. Thus, So does not disclose all of the limitations of

claims 1, 11 and 21, and thus So does not anticipate claims 1, 11 and 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "a plurality of digital signal processing (DSP) units" as recited in claim 21. The Examiner has not specifically addressed this limitation. In order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 21. M.P.E.P. §2131.

Furthermore, Appellants respectfully assert that So does not disclose "a direct memory access controller coupled to said plurality of DSP processor cores" as recited in claim 21. The Examiner cites element 316 in Figure 3 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 9. Appellants respectfully traverse. Element 316 in Figure 3 of So does disclose a DMA control circuit. However, element 316 of So is not coupled to a plurality of DSP processor cores. Thus, So does not disclose all of the limitations of claim 21, and thus So does not anticipate claim 21. M.P.E.P. §2131.

Appellants further assert that So does not disclose "wherein said direct memory access controller comprises: a memory unit operable for storing a computer program for facilitating inter-DSP data communications; and a processor coupled to said memory unit, wherein said processor, responsive to said computer program" as recited in claim 21. As stated above, the Examiner cites element 316 in Figure 3 of So as disclosing a direct memory access controller. However, the Examiner now relies upon elements 102, 104, 112 of Figure 2 and column 9, lines 51-62 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 9. Elements 102, 104, 112 relate to a CPU, a cache and memory of a personal computer and not to a memory unit and processor of a direct memory access controller (which

the Examiner asserts as being disclosed by element 316 in Figure 3 of So). Thus, So does not disclose all of the limitations of claim 21, and thus So does not anticipate claim 21. M.P.E.P. §2131.

B. Claims 2-10, 12-20 and 22-30 are not anticipated by So for at least the reasons that claims 1, 11 and 21, respectively, are not anticipated by So.

Claims 2-10 each recite combinations of features of independent claim 1, and hence claims 2-10 are not anticipated by So for at least the reasons that claim 1 is not anticipated by So.

Claims 12-20 each recite combinations of features of independent claim 11, and hence claims 12-20 are not anticipated by So for at least the reasons that claim 11 is not anticipated by So.

Claims 22-30 each recite combinations of features of independent claim 21, and hence claims 22-30 are not anticipated by So for at least the reasons that claim 21 is not anticipated by So.

C. Claims 2, 12 and 22 are not anticipated by So.

Appellants respectfully assert that So does not disclose "obtaining a pointer to a second data structure from said first data structure" as recited in claim 2 and similarly in claims 12 and 22. The Examiner cites the "linked list" in Figure 22 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 3. The Examiner further states that it is well known in the art for a linked list to include data structure entries which point from a preceding structure to a subsequent structure. *Id.* Appellants respectfully traverse. A linked list is a group of items, each of which points to the next item. *See www.techweb.com/encyclopedia.* However, there is no language in So that describes the linked list referred to in Figure 22 as disclosing the aspect of obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core. Instead, Figure 22 illustrates a table of region lists which are not data structures

associated with local memories of DSP processor cores. Thus, So does not disclose all of the limitations of claims 2, 12 and 22, and thus So does not anticipate claims 2, 12 and 22. M.P.E.P. §2131.

Further, in connection with the rejection of the above-cited claim limitation, Appellants respectfully assert that the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that So inherently discloses obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that So inherently discloses obtaining a pointer to a second data structure from a first data structure associated with a block of local memory in a first DSP processor core, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 2, 12 and 22.

Appellants further assert that So does not disclose "reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer" as recited in claim 2 and similarly in claims 12 and 22. The Examiner cites column 16, lines 8-18 and Figure 21 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 3. Appellants respectfully traverse. As stated above, So instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. So further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, So discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses reading a second

data structure. Neither is there any language in the cited passage that discloses reading a second data structure, where the second data structure includes a second source address of one of a read pointer and a write pointer. Neither is there any language in the cited passage that discloses reading a second data structure, where the second data structure includes a second destination address of one of the read pointer and the write pointer. Thus, So does not disclose all of the limitations of claims 2, 12 and 22, and thus So does not anticipate claims 2, 12 and 22. M.P.E.P. §2131.

D. Claims 3, 13 and 23 are not anticipated by So.

Appellants respectfully assert that So does not disclose "initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core" as recited in claim 3 and similarly in claims 13 and 23. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 3. Appellants respectfully traverse. As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that disclose initiating a transfer of a write pointer located in a second source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a write pointer located in a second source address in the local memory of the first DSP processor core to the second destination address in the local memory of the second DSP processor core. Thus, So does not disclose all of the limitations of claims 3, 13 and 23, and thus So does not anticipate claims 3, 13 and 23. M.P.E.P. §2131.

E. Claims 4, 14 and 24 are not anticipated by So.

Appellants respectfully assert that So does not disclose "initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core" as recited in claim 4 and similarly in claims 14 and 24. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 4. Appellants respectfully traverse. As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of a read pointer located in the second source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a read pointer located in the second source address in the local memory of the second DSP processor core to the second destination address in the local memory of the first DSP processor core. Thus, So does not disclose all of the limitations of claims 4, 14 and 24, and thus So does not anticipate claims 4, 14 and 24. M.P.E.P. §2131.

F. Claims 5, 15 and 25 are not anticipated by So.

Appellants respectfully assert that So does not disclose "obtaining a pointer to a third data structure from said second data structure" as recited in claim 5 and similarly in claims 15 and 25. The Examiner cites the "linked list" in Figure 22 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 4. Appellants respectfully traverse. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the statement of "linked list" in Figure 22 of So inherently discloses obtaining a pointer to a third data structure from a second data structure. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the statement of "linked list" in Figure 22 of So inherently discloses

obtaining a pointer to a third data structure from a second data structure, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 5, 15 and 25. M.P.E.P. §2131.

Appellants further assert that So does not disclose "reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer" as recited in claim 5 and similarly in claims 15 and 25. The Examiner cites column 16, lines 8-18 and Figure 21 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 4. Appellants respectfully traverse. As stated above, So instead discloses that the CPU provides pointer addresses to the main memory. Column 16, line 8. So further discloses that the three addresses needed are the base address for the DSP's 128K bytes of program space, the 128K bytes of read data space (source), and the 128K bytes of write data space (destination). Column 16, lines 9-12. Additionally, So discloses that depending on the application, these may point to different areas of memory, or point to the same area of memory. Column 16, lines 12-14. There is no language in the cited passage that discloses reading a third data structure. Neither is there any language in the cited passage that discloses reading a third data structure, where the third data structure includes a third source address of one of a read pointer and a write pointer. Neither is there any language in the cited passage that discloses reading a third data structure, where the third data structure includes a third destination address of one of the read pointer and the write pointer. Thus, So does not disclose all of the limitations of claims 5, 15 and 25, and thus So does not anticipate claims 5, 15 and 25. M.P.E.P. §2131.

G. Claims 6, 16 and 26 are not anticipated by So.

Appellants respectfully assert that So does not disclose "initiating a transfer of

said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core" as recited in claim 6 and similarly in claims 16 and 26. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 4. Appellants respectfully traverse.

As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of a write pointer located in the second source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of a write pointer located in the second source address in the local memory of the first DSP processor core to the second destination address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the third source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the third source address in the local memory of the second DSP processor core to the third destination address in the local memory of the first DSP processor core. Thus, So does not disclose all of the limitations of claims 6, 16 and 26, and thus So does not anticipate claims 6, 16 and 26. M.P.E.P. §2131.

H. Claims 7, 17 and 27 are not anticipated by So.

Appellants respectfully assert that So does not disclose "initiating a transfer of said write pointer located in said third source address in said local memory of said

first DSP processor core to said third destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core" as recited in claim 7 and similarly in claims 17 and 27. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 5. Appellants respectfully traverse.

As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses initiating a transfer of the write pointer located in the third source address in the local memory of the first DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the write pointer located in the third source address in the local memory of the first DSP processor core to the third destination address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the second source address in the local memory of the second DSP processor core. Neither is there any language in the cited passage that discloses initiating a transfer of the read pointer located in the second source address in the local memory of the second DSP processor core to the second destination address in the local memory of the first DSP processor core. Thus, So does not disclose all of the limitations of claims 7, 17 and 27, and thus So does not anticipate claims 7, 17 and 27. M.P.E.P. §2131.

I. Claims 8, 18 and 28 are not anticipated by So.

Appellants respectfully assert that So does not disclose "converting a local address of said write pointer to a global address" as recited in claim 8 and similarly in claims 18 and 28. The Examiner cites column 19, lines 1-11 of So as disclosing the

above-cited claim limitation. Office Action (11/7/2006), page 5. Appellants respectfully traverse and assert that So instead discloses that the PCI address offset is the address in DSP space which will be translated into PCI space and used to transfer data from or to the host. Column 19, lines 1-3. There is no language in the cited passage that discloses converting a local address of the writer pointer (contained in the second data structure) to a global address. Thus, So does not disclose all of the limitations of claims 8, 18 and 28, and thus So does not anticipate claims 8, 18 and 28. M.P.E.P. §2131.

Appellants further assert that So does not disclose "computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer" as recited in claim 8 and similarly in claims 18 and 28. The Examiner cites column 23, lines 1-7 and 23-24 of So as well as Figure 24 as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 5. Appellants respectfully traverse and assert that So instead discloses that for every transaction there is also known where the source and destination table is. Column 23, lines 1-2. So further discloses that Figure 24 is a detail of a region list for the source data DMA transfer table. Column 23, lines 23-24. There is no language in the cited passages that discloses computing the first source address in the first data structure. Neither is there any language in the cited passages that discloses computing the first source address in the first data structure, where the first source address is equal to the size of a block of memory subtracted from the global address of the write pointer. Thus, So does not disclose all of the limitations of claims 8, 18 and 28, and thus So does not anticipate claims 8, 18 and 28. M.P.E.P. §2131.

J. Claims 9, 19 and 29 are not anticipated by So.

Appellants respectfully assert that So does not disclose "reading said local address of said write pointer; and copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core" as recited in

claim 9 and similarly in claims 19 and 29. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 5. Appellants respectfully traverse. As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses reading the local address of the write pointer. Neither is there any language in the cited passage that discloses copying the local address of the write pointer. Neither is there any language in the cited passage that discloses copying the local address of the write pointer into an entry in a third data structure located in the first DSP processor core. Thus, So does not disclose all of the limitations of claims 9, 19 and 29, and thus So does not anticipate claims 9, 19 and 29. M.P.E.P. §2131.

K. Claims 10, 20 and 30 are not anticipated by So.

Appellants respectfully assert that So does not disclose "reading a local address of said read pointer; and copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core" as recited in claim 10 and similarly in claims 20 and 30. The Examiner cites column 13, lines 1-23 of So as disclosing the above-cited claim limitation. Office Action (11/7/2006), page 5. Appellants respectfully traverse. As stated above, So instead discloses that Windows has an architecture that calls for handles like a file drawer that tell where in virtual memory the software starts and ends. Column 13, lines 1-3. So further discloses that they provide a mechanism to locate memory resources in virtual memory space. Column 13, lines 3-4. There is no language in the cited passage that discloses reading a local address of the read pointer. Neither is there any language in the cited passage that discloses copying the local address of the read pointer. Neither is there any language in the cited passage that discloses copying the local address of the read pointer into an entry in a third data structure located in the second DSP processor core. Thus, So does not disclose all of the limitations of claims 10, 20 and

30, and thus So does not anticipate claims 10, 20 and 30. M.P.E.P. §2131.

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-30 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-30.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method for facilitating inter-digital signal processing (DSP) data communications comprising the steps of:

reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

2. The method as recited in claim 1 further comprising the steps of:

obtaining a pointer to a second data structure from said first data structure;

reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

3. The method as recited in claim 2 further comprising the step of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

4. The method as recited in claim 2 further comprising the step of:

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination

address in said local memory of said first DSP processor core.

5. The method as recited in claim 2 further comprising the steps of:

obtaining a pointer to a third data structure from said second data structure;

reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

6. The method as recited in claim 5 further comprising the steps of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

7. The method as recited in claim 5 further comprising the steps of:

initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

8. The method as recited in claim 2 further comprising the steps of:

converting a local address of said write pointer to a global address; and

computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

9. The method as recited in claim 8 further comprising the steps of:

reading said local address of said write pointer; and

copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

10. The method as recited in claim 8 further comprising the steps of:

reading a local address of said read pointer; and

copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.

11. A computer program product embodied in a machine readable medium for facilitating inter-digital signal processing (DSP) data communications comprising the programming steps of:

reading a first data structure associated with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

12. The computer program product as recited in claim 11 further comprising the programming steps of:

obtaining a pointer to a second data structure from said first data structure;

reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer,

wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

13. The computer program product as recited in claim 12 further comprising the programming step of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

14. The computer program product as recited in claim 12 further comprising the programming step of:

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

15. The computer program product as recited in claim 12 further comprising the programming steps of:

obtaining a pointer to a third data structure from said second data structure;

reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

16. The computer program product as recited in claim 15 further comprising the programming steps of:

initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

17. The computer program product as recited in claim 15 further comprising the programming steps of:

initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

18. The computer program product as recited in claim 12 further comprising the programming steps of:

converting a local address of said write pointer to a global address; and

computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

19. The computer program product as recited in claim 18 further comprising the programming steps of:

reading said local address of said write pointer; and

copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

20. The computer program product as recited in claim 18 further comprising the steps of:

reading a local address of said read pointer; and

copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.

21. A system, comprising:

a plurality of digital signal processing (DSP) units;

a direct memory access controller coupled to said plurality of DSP processor

cores, wherein said direct memory access controller comprises:

a memory unit operable for storing a computer program for facilitating inter-DSP data communications; and

a processor coupled to said memory unit, wherein said processor, responsive to said computer program, comprises:

circuitry operable for reading a first data structure associated with a block of local memory in a first DSP processor core, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core, wherein said first data structure further comprises an indication of a size of a block of memory, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core; and

circuitry operable for initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core.

22. The system as recited in claim 21, wherein said processor further comprises:

circuitry operable for obtaining a pointer to a second data structure from said first data structure;

circuitry operable for reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer.

23. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core.

24. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

25. The system as recited in claim 22, wherein said processor further comprises:

circuitry operable for obtaining a pointer to a third data structure from said second data structure;

circuitry operable for reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer.

26. The system as recited in claim 25, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and

circuitry operable for initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core.

27. The method as recited in claim 25, wherein said processor further comprises:

circuitry operable for initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and

circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core.

28. The system as recited in claim 22, wherein said first DSP processor core

comprises:

a second memory unit operable for storing a computer program for performing background tasks; and

a second processor coupled to said second memory unit, wherein said second processor, responsive to said computer program, comprises:

circuitry operable for converting a local address of said write pointer to a global address; and

circuitry operable for computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer.

29. The system as recited in claim 28, wherein said second processor further comprises:

circuitry operable for reading said local address of said write pointer; and

circuitry operable for copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core.

30. The system as recited in claim 28, wherein said second DSP processor core comprises:

a third memory unit operable for storing a computer program for performing background tasks; and

a third processor coupled to said third memory unit, wherein said third processor, responsive to said computer program, comprises:

circuitry operable for reading a local address of said read pointer; and

circuitry operable for copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.

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